# PC104-DAS08

# User's Manual

Revision 4

September, 2001

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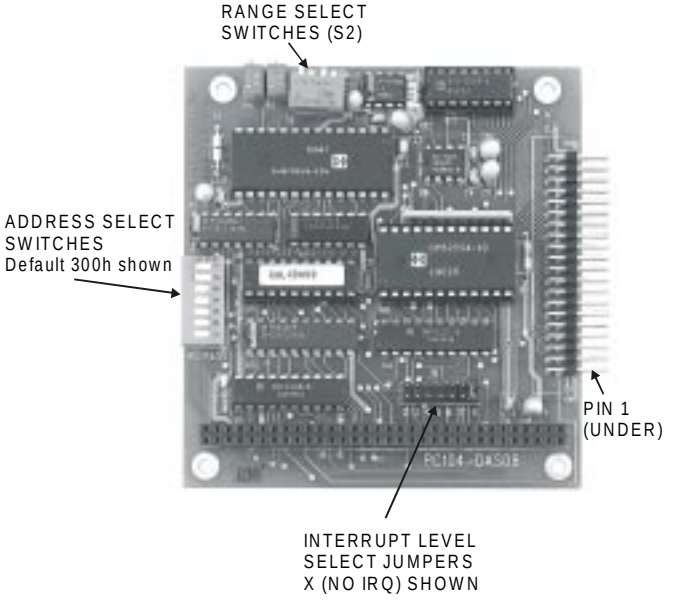
# 1 INSTALLATION

## 1.1 SOFTWARE INSTALLATION

Before you open your computer and install the board, install and run *Insta*Cal, the installation, calibration and test utility included with your board. *Insta*Cal will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. Refer to the *Software Installation Manual* for *Insta*Cal installation instructions.

## 1.2 HARDWARE INSTALLATION

The PC104-DAS08 has three sets of switches / jumpers that should be set before installing the board in the PC. There is a bank of DIP switches for setting the base address, a jumper for setting the interrupt level and a bank of switches for setting the




analog input range. See Figure 1-1 below.

Figure 1-1. Switch and Jumper Locations

## 1.2 .1 Setting the Base Address Switches

Select a base address from those available in your system. The PC104-DAS08 uses eight addresses.

Set the switches on your base address switch as shown on the diagram. Unless there is already a board in your system using address 300 hex (768 decimal), leave the switches as they are set at the factory.

In the example shown in Figure 1-2, the switches are set for base address 300h.

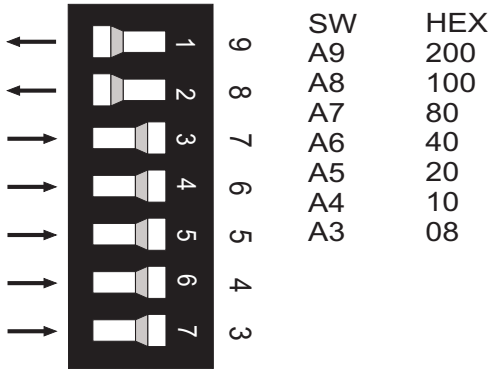



Figure 1-2. Base Address Switch

Certain addresses are used by the PC, others are free and may be used by the PC104-DAS08 and other expansion boards. Refer to Table 1-1 for PC addresses.

Table 1-1. PC I/O Addresses

| HEX RANGE | FUNCTION | HEX RANGE | FUNCTION |
|---|---|---|---|
| 000-00F | 8237 DMA #1 | 2C0-2CF | EGA |
| 020-021 | 8259 PIC #1 | 2D0-2DF | EGA |
| 040-043 | 8253 TIMER | 2E0-2E7 | GPIB (AT) |
| 060-063 | 8255 PPI (XT) | 2E8-2EF | SERIAL PORT |
| 060-064 | 8742 CONTROLLER (AT) | 2F8-2FF | SERIAL PORT |
| 070-071 | CMOS RAM & NMI MASK (AT) | 300-30F | PROTOTYPE CARD |
| 080-08F | DMA PAGE REGISTERS | 310-31F | PROTOTYPE CARD |
| 0A0-0A1 | 8259 PIC #2 (AT) | 320-32F | HARD DISK (XT) |
| 0A0-0AF | NMI MASK (XT) | 378-37F | PARALLEL PRINTER |
| 0C0-0DF | 8237 #2 (AT) | 380-38F | SDLC |
| 0F0-0FF | 80287 NUMERIC CO-P (AT) | 3A0-3AF | SDLC |
| 1F0-1FF | HARD DISK (AT) | 3B0-3BB | MDA |
| 200-20F | GAME CONTROL | 3BC-3BF | PARALLEL PRINTER |
| 210-21F | EXPANSION UNIT (XT) | 3C0-3CF | EGA |
| 238-23B | BUS MOUSE | 3D0-3DF | CGA |
| 23C-23F | ALT BUS MOUSE | 3E8-3EF | SERIAL PORT |
| 270-27F | PARALLEL PRINTER | 3F0-3F7 | FLOPPY DISK |
| 2B0-2BF | EGA | 3F8-3FF | SERIAL PORT |

The BASE switches can be set for address in the range of 000-3F8 so it should not be hard to find a free address area. If you are not using IBM prototyping cards, 300-31F HEX are free to use.

Address not specifically listed, such as 390-39F, are free.

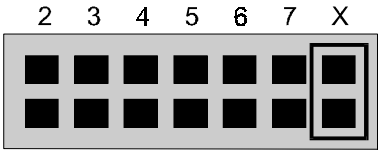
## 1.2 .2 INTERRUPT LEVEL SELECT

The interrupt jumper need only be set if the software you are using requires it. If you do set the interrupt jumper, please check your PC's current configuration for interrupt conflicts.

Do not use IR2 in PC/AT class machines (or higher).

There is a jumper block on the PC104-DAS08 located just above the PC bus interface (see Figure 1-1). The factory default setting is that no interrupt level is set (the jumper is in the 'X' position). See Figure 1-3.

If you need to pace conversions through hardware (either the on-board pacer or an external clock), move this jumper to one of the other positions (see Table 1-2).




**INTERRUPT JUMPER BLOCK - Jumper in X position = No IRQ.**

Figure 1-3. Interrupt Jumper Block

Table 1-2. IRQ Assignments

| NAME | DESCRIPTION | NAME | DESCRIPTION |
|---|---|---|---|
| NMI | PARITY | IRQ8 | REAL TIME CLOCK (AT) |
| IRQ0 | TIMER | IRQ9 | RE-DIRECTED TO IRQ2 (AT) |
| IRQ1 | KEYBOARD | IRQ10 | UNASSIGNED |
| IRQ2 | RESERVED (XT)<br>INT 8-15 (AT) | IRQ11 | UNASSIGNED |
| IRQ3 | COM OR SDLC | IRQ12 | UNASSIGNED |
| IRQ4 | COM OR SDLC | IRQ13 | 80287 NUMERIC CO-P |
| IRQ5 | HARD DISK (AT)<br>LPT (AT) | IRQ14 | HARD DISK |
| IRQ6 | FLOPPY DISK | IRQ15 | UNASSIGNED |
| IRQ7 | LPT | Note: IRQ8-15 are AT only | |

## 1.2 .3 RANGE SWITCH SETTING

The DIP switch labeled S2 controls the range (gain) settings for both bipolar ranges (±5V and ±10V), and for the unipolar range (0 to 10V). For location, see Figure 1-1. Switch S2 has four ganged switches to select an input range for the analog inputs (Figure 1-4).

Refer to Table 1-3 to determine the correct positions of switches S2-1 through S2-4 for the range you desire.

These switches control the analog input range for all eight channels.

Table 1-3. Range Select Switch (S2) Settings

| S1 | S2 | S3 | S4 | **GAIN** | **RANGE** | **RESOLUTION** |
|---|---|---|---|---|---|---|
| Up | Down | Up | Down | 1 | ±5V | 2.44mV / bit |
| Down | Up | Up | Down | 0.5 | ±10V | 4.88mV / bit |
| Up | Down | Down | Up | 1 | 0 to 10V | 2.44mV / bit |

NOTE: Up = open; Down = closed.

Positions other than those listed are not valid.

The PC104-DAS08 is ready to test. You can try running the software supplied with your board now, or you can continue reading the next section on Software Installation and Calibration.

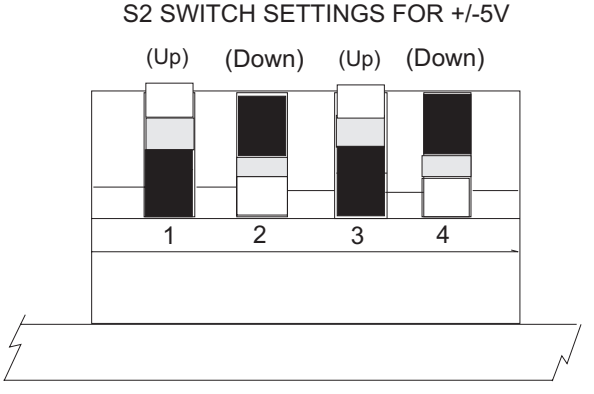



Figure 1-4. Range Select Switch S2

# 2 SIGNAL CONNECTIONS

## 2.1 CONNECTOR DIAGRAMS

The PC104-DAS08 analog connector is a 40-pin header connector.

The connector accepts female 40-pin header connectors, such as those on the C40FF-2, 2 foot cable with connectors. If connector compatibility with a CIO-DAS08 is required, the C40-37F-# or BP40-37 adapter cables can be used. The C40-37F-# cable converts the signals on the 40-pin header into the standard DAS08 37-pin, D connector pin assignments. If a connector on a standard PC bracket is required, the BP40-37 adapter cable can be used to convert the 40-pin female header to a 37-pin male mounted on a bracket. See Figure 2-2 for the BP40-37 pinout.

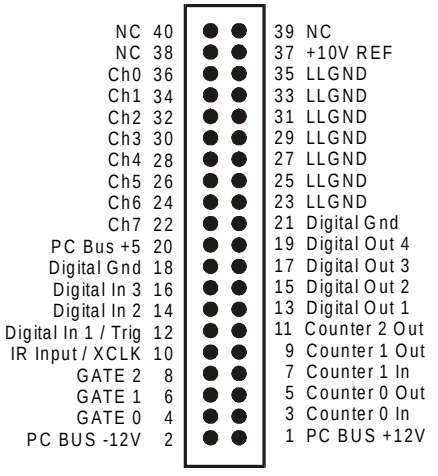



Figure 2-1. Analog Connector

Figure 2-3 shows the cabling of the BP-40-37..

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL and CIO-MINI37 screw terminal boards, CIO-EXP32, 32 channels analog MUX/AMP or the ISO-RACK08, 8-position 5B module interface rack.

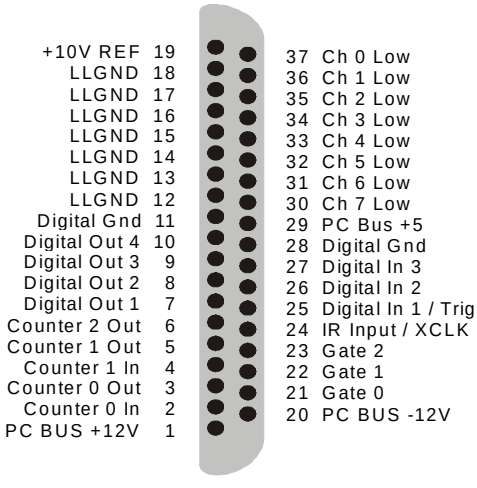



Figure 2-2. BP40-37 Adapter Cable Pinout

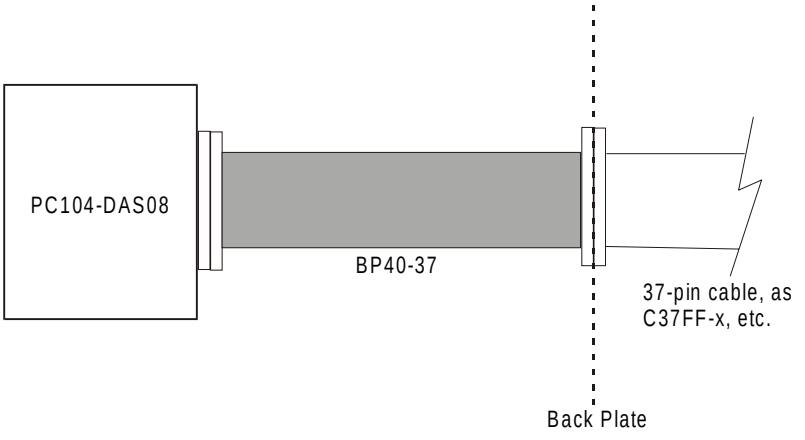



Figure 2-3. BP40-37 Adapter Cabling

## 2.2 ANALOG INPUTS

Analog inputs to the PC104-DAS08 are single-ended.

**CAUTION - PLEASE READ**

Measure the voltage between signal ground at the signal source and the PC's ground. If the voltage exceeds 0.5V (AC or DC), DO NOT CONNECT the PC104-DAS08 to this signal source because you will not be able to make an accurate measurement.

Voltage between the two grounds means that you will create a ground loop if you connect the signal ground to the PC104-DAS08 board ground. Current flow in the ground loop can damage the board and possibly the computer.

## 2.3 SINGLE-ENDED INPUTS

A single-ended input is two wires connected to the board, a channel high (CH# HI) and a Low Level Ground (LLGND). The LLGND signal must be the same ground the PC is on. The CH# HI is the voltage signal source. There is no common mode rejection on a single-ended input so shielding and proper grounding is important both for voltage differentials and for noise immunity. If greater amplification or expanded differential inputs are required, we suggest using a CIO-EXP32, 32 channel or CIO-EXP16, 16-channel analog input multiplexer and amplifier.

# 3 REGISTER ARCHITECTURE

## 3.1 CONTROL & DATA REGISTERS

The PC104-DAS08 is controlled and monitored by writing to and reading from eight consecutive 8-bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Most often, register manipulation is best left to experienced programmers as most of the PC104-DAS08 possible functions are implemented in easy to use Universal Library functions.

The register descriptions follow the format:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A/D9 | A/D10 | A/D11 | A/D12<br>LSB | CH8 | CH4 | CH2 | CH1 |

Numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the weights in Table 3-1 apply:

Table 3-1. Bit Weights

| BIT POSITION | DECIMAL VALUE | HEX VALUE |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 2 | 2 |
| 2 | 4 | 4 |
| 3 | 8 | 8 |
| 4 | 16 | 10 |
| 5 | 32 | 20 |
| 6 | 64 | 40 |
| 7 | 128 | 80 |

To write control words or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte.

The method of programming required to set/read bits from bytes is beyond the scope of this manual.

In summary form, the registers and their function are listed on Table 4-2. Within each register are eight bits which either constitute a byte of data or eight individual bit set/read functions.

Table 3-2. Board Registers

| ADDRESS | READ FUNCTION | WRITE FUNCTION |
|---|---|---|
| BASE | A/D Bits 9-12(LSB) | Start 8 bit A/D conversion |
| BASE + 1 | A/D Bits 1(MSB)-8 | Start 12 bit A/D conversion |
| BASE + 2 | EOC, IP1-IP3, IRQ, MUX Address | OP1-OP4, INTE & MUX Address |
| BASE + 3 | Not used | Not used |
| BASE + 4 | Read Counter 0 | Load Counter 0 |
| BASE + 5 | Read Counter 1 | Load Counter 1 |
| BASE + 6 | Read Counter 2 | Load Counter 2 |
| BASE + 7 | Not used | Counter Control |

## 3.2 A/D DATA REGISTER

BASE ADDRESS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A/D9 | A/D10 | A/D11 | A/D12 LSB | 0 | 0 | 0 | 0 |

A read/write register.

READ

On read, it contains the least significant four digits of the analog input data.

These four bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, forming a complete 12-bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

WRITE

Writing any data to the register causes an immediate 8-bit A/D conversion.

BASE ADDRESS + 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A/D1 MSB | A/D2 | A/D3 | A/D4 | A/D5 | A/D6 | A/D7 | A/D8 |

READ

On read the most significant A/D byte is read.

The A/D Bits code corresponds to the voltage on the input according to Table 4-3.

Table 3-3. A/D Bit Codes

| DECIMAL | HEX | BIPOLAR | UNIPOLAR |
|---|---|---|---|
| 4095 | FFF | + Full Scale | +Full Scale |
| 2048 | 800 | 0 Volts | ½ Full Scale |
| 0 | 0 | –Full Scale | 0 Volts |

WRITE

Writing to this register starts a 12-bit A/D conversion.

Note: Place several NO-OP instructions between consecutive 12-bit A/D conversions to avoid over-running the A/D converter.

## 3.3 STATUS AND CONTROL REGISTER

BASE ADDRESS + 2

This register address is two registers, one is read active and one is write active.

READ = STATUS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EOC | IP3 | IP2 | IP1 | IRQ | MUX2 | MUX1 | MUX0 |

EOC = 1 the A/D is busy converting and data should not be read.

EOC = 0 the A/D is not busy and data may be read.

IP3 to IP1 are the digital input lines.

IRQ is the status of an edge triggered latch connected to the “Interrupt Req” pin on the analog connector. It is high (1) when a positive edge has been detected. It may be reset to 0 by writing to the INTE mask at BASE + 2 write.

MUX 2 to MUX 0 is the current multiplexer channel. The current channel is a binary coded number between 0 and 7 .

WRITE = CONTROL

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OP4 | OP3 | OP2 | OP1 | INTE | MUX2 | MUX1 | MUX0 |

OP4 to OP1 are the digital output lines.

INTE = 1 enables interrupts (positive edge triggered) onto the PC bus IRQ selected via the IRQ jumper on the PC104-DAS08.

INTE = 0 disables the passing of the interrupt detected at pin 10 to the PC bus.

IRQ is set to 1 every time an interrupt occurs. If you want to process successive interrupts then set INTE = 1 as the last step in your interrupt service routine.

MUX2 to MUX0. Set the current channel address by writing a binary coded number between 0 and 7 to these three bits.

**NOTE**

Every write to this register sets the current A/D channel MUX setting to the number in bits 2-0.

## 3.4 UNUSED ADDRESS

BASE ADDRESS + 3

This address is not used

## 3.5 COUNTER LOAD & READ REGISTERS

COUNTER 0

BASE ADDRESS + 4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

COUNTER 1

BASE ADDRESS + 5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

COUNTER 2

BASE ADDRESS + 6

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

The data in the counter read register, and the action taken on the data in a counter load register, is dependent upon the control code written to the control register.

The counters are 16-bit types, each with an 8-bit window (the read / load register). Data is shifted into and out of the 16-bit counters through these 8-bit windows according to the control byte. You will need an 8254 data sheet if you want to program the 8254 directly at the register level. You can download a copy from our WEB site at http://www.computerboards.com/PDFmanuals/82C54.pdf

## 3.6 COUNTER CONTROL REGISTER

BASE ADDRESS + 7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |

WRITE ONLY

SC1 to SC0 are the counter-select bits. They are binary coded between 0 and 2.

RL1 to RL0 are the read and load control bits:

| **RL1** | **RL0** | **OPERATION** |
|---|---|---|
| 0 | 0 | Latch counter. |
| 0 | 1 | Read/load high byte. |
| 1 | 0 | Read/load low byte. |
| 1 | 1 | Read/load low the high byte (word transfer). |

M2 to M0 are the counter control operation type bits:

| **M2** | **M1** | **M0** | **OPERATION TYPE** |
|---|---|---|---|
| 0 | 0 | 0 | Change on terminal count. |
| 0 | 0 | 1 | Programmable one-shot. |
| 0 | 1 | 0 | Rate generator |
| 0 | 1 | 1 | Square wave generator |
| 1 | 0 | 0 | Software triggered strobe. |
| 1 | 0 | 1 | Hardware triggered strobe. |

If BCD = 0, then counter data is 16-bit binary. (65,535 max)

If BCD = 1, then counter data is 4-decade Binary Coded Decimal. (9,999 max)

# 3.7 COUNTER TIMER

The 82C54 counter timer chip can be used for event counting, frequency and pulse measurement and as a pacer clock for the A/D converter. Several of the Universal Library A/D routines assume that counter 2, which is hard-wired to the PC bus signal PCLK, is pacing the A/D samples. All inputs, outputs and gates of the counter are accessible at the 40 pin analog connector with the exception of the counter 2 input.

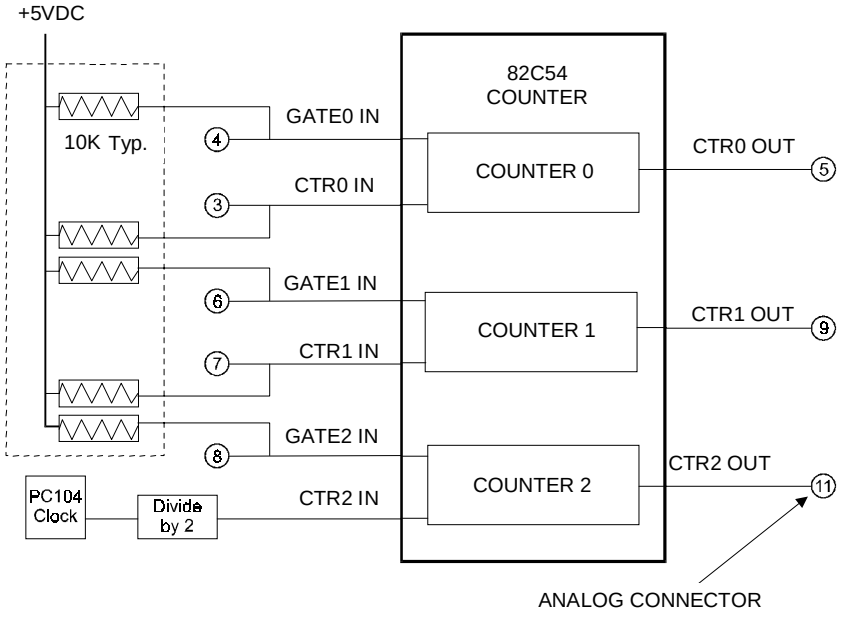



Figure 3-1. 82C54 Counter Block Diagram

The primary purpose of the counter timer chip is to pace the A/D samples. The input to Counter 2 is hard-wired to the PC bus PCLK signal so that a precise timing signal will always be available on the board. The counter gates, inputs and outputs are TTL.

The counter GATE2 IN line allows or inhibits TTL level pulses present at the CLK input into the counter 2 register. The OUT line then transitions (pulses or shifts) depending on the codes in the control register.

The PCLK signal is divided by two prior to the input at counter 2. Therefore, if the PCLK signal on your PC/AT is 8 MHz, the signal at the input of counter 2 is 4 MHz.

Assuming a 4 MHz signal at counter 2, the rates out of counter 2 (pin 11) can vary between 2 MHz (4 MHz / 2) to 61 Hz (4 MHz / 65,535). For rates slower than 61 Hz the output of counter 2 should be wired to the input of counter 1. The output of

counter 1 would then be wired to the interrupt input (pin 10). The slowest rate would then be once every 17 minutes.

## 3.8 DIGITAL INPUT

The digital inputs are TTL-level lines. They feed an 8-bit register which has other on-board signals applied to it. The resultant 8-bit status byte can be read at BASE address + 2.

The digital inputs IP1, IP2 & IP3 can be used as status lines to trigger or hold off A/D conversions, and in fact, the Universal Library uses IP1 for that purpose.

## 3.9 DIGITAL OUTPUT

The digital output lines, OP1, OP2, OP3 & OP4 are TTL level lines which are controlled with part of an 8-bit register located at BASE address + 2. These lines may be used to control the multiplexer address on an external CIO-EXP32 differential amplifier/ multiplexer if one is installed.

## 3.10 TRIGGER & INTERRUPT LOGIC

The trigger logic works as follows: The INTERRUPT REQ signal on Pin 10 of the 40-pin connector is an input to a flip-flop. It can be read at BASE address + 2 on the IRQ bit. The PC104-DAS08 can be triggered by polling this bit until a trigger pulse (rising edge) has occurred. It must be reset by a write to BASE + 2 before it can respond to additional rising edges.

By writing a 1 to the INTE control bit at BASE + 2, the rising edge detected by the flip-flop will be translated into an interrupt pulse which can be used to interrupt the CPU's 8259 interrupt controller on the PC motherboard.

The interrupt level jumper on the PC104-DAS08 must also be installed. Move it from the 'X' position to the IRQ number you want the interrupt pulse on.

The 82C54 counter/timer chip is primarily a pacer for A/D samples. It is an integral part of the trigger logic. To employ the 82C54 as an A/D pacer, wire the output of the counter you program to provide pacing pulses directly into the INTERRUPT REQ input (pin 10).

# 4 SPECIFICATIONS

**Power Consumption**

| | |
|---|---|
| +5V: | 130 mA typical, 185 mA max |
| +12V: | 18 mA typical, 25 mA max |
| –12V: | 12 mA typical, 18 mA max |

**Analog Input Section**

| | |
|---|---|
| A/D converter type | AD674 |
| Resolution | 12 bits |
| Number of channels | 8, single-ended |
| Input Ranges | ±10V, ±5V, 0 to +10V, switch selectable |
| Polarity | Unipolar/Bipolar, switch selectable |
| A/D pacing | Internal counter or external source (Interrupt Input, jumper selectable, rising edge) or software polled |
| A/D Trigger sources | External polled gate trigger (Digital In 1) |
| Data transfer | Interrupt or software polled |
| DMA | None |
| A/D conversion time | 15 µs |
| Throughput | 20 kHz, PC dependent |
| Accuracy | ±0.01% of reading ±1 LSB |
| Differential Linearity error | ±1 LSB |
| Integral Linearity error | ±0.5 LSB |
| No missing codes guaranteed | 12 bits |
| Gain drift (A/D specs) | ±25 ppm/°C |
| Zero drift (A/D specs) | ±10µV/°C |
| Common Mode Range | ±10V |
| CMRR | 72 dB |
| Input leakage current (@25 Deg C) | 100 nA |
| Input impedance | 10 MegOhms min |
| Absolute maximum input voltage | ±35V |

**Digital Input / Output**

| | |
|---|---|
| Digital Type (Main connector) | |
| Output: | 74LS273 |
| Input: | 74LS244 |
| Configuration | 4 fixed output bits, 3 fixed input bits |
| Number of channels | 4 out, 3 in |
| Output High | 2.7 volts min @ –0.4 mA |
| Output Low | 0.4 volts max @ 8 mA |
| Input High | 2.0 volts min, 7 volts absolute max |
| Input Low | 0.8 volts max, –0.5 volts absolute min |
| Output power-up / reset state | |
| Interrupts | 2 thru 7, jumper-selectable |
| Interrupt enable | Programmable |
| Interrupt sources | External (Interrupt In), rising edge |

**Counter Section**

| | |
|---|---|
| Counter type | 82C54 |
| Configuration | 3 down-counters, 16 bits each |
| | Counter 0 - independent, user configurable |
| | Source: user connector (Counter 0 In) |
| | Gate: user connector (Gate 0) |
| | Output: user connector (Counter 0 Out) |
| | Counter 1 - independent, user configurable |
| | Source: user connector (Counter 1 In) |
| | Gate: user connector (Gate 1) |
| | Output: user connector (Counter 1 Out) |
| | Counter 2 - independent, user configurable |
| | Source: PC SysClk via divide by 2 circuit |
| | Gate: user connector (Gate 2) |
| | Output: user connector (Counter 2 Out) |
| Clock input frequency | 10 MHz max |
| High pulse width (clock input) | 30 ns min |
| Low pulse width (clock input) | 50 ns min |
| Gate width high | 50 ns min |
| Gate width low | 50 ns min |
| Input low voltage | 0.8V max |
| Input high voltage | 2.0V min |
| Output low voltage | 0.4V max |
| Output high voltage | 3.0V min |

**Environmental**

| | |
|---|---|
| Operating temperature range | 0 to 50°C |
| Storage temperature range | –20 to 70°C |
| Humidity | 0 to 90% non-condensing |

**For Your Notes**

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**EC Declaration of Conformity**

We, Measurement Computing Corporation, declare under sole responsibility that the product:

| Part Number | Description |
|---|---|
| PC104-DAS08 | Analog Input, DI/O and Counter card |

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

**EU EMC Directive 89/336/EEC**: Essential requirements relating to electromagnetic compatibility.

**EU 55022 Class B**: Limits and methods of measurements of radio interference characteristics of information technology equipment.

**EN 50082-1**: EC generic immunity requirements.

**IEC 801-2**: Electrostatic discharge requirements for industrial process measurement and control equipment.

**IEC 801-3**: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

**IEC 801-4**: Electrically fast transients for industrial process measurement and control equipment.

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